(12) UK Patent Application (19) GB (11) 2 174 543 A

(43) Application published 5 Nov 1986

(21) Application No 8609260

(22) Date of filing 16 Apr 1986

(30) Priority data

(31) 20504 (32) 26 Apr 1985 (33) IT

(51) INT CL[4]
H01L 23/50

(52) Domestic classification (Edition H):
H1K 4C11 4C1U 4F13 4F18 RG

(56) Documents cited
GB 1173117

(58) Field of search
H1K
Selected US specifications from IPC sub-class H01L

(71) Applicant
SGS Microelettronica SpA (Italy),
Stradale Primosole 50, 95121 Catania, Italy

(72) Inventor
Carlo Cognetti de Martiis

(74) Agent and/or Address for Service
Marks & Clerk, 57-60 Lincoln's Inn Fields,
London WC2A 3LS

(54) Improved packaging of semiconductor devices

(57) In a package (20) containing a semiconductor or an integrated circuit chip (10), an insulating layer (12) is deposited on the chip (10), and a group of electrodes (13) are deposited on the insulating layer (12). The group of electrodes (13) are generally larger than the internal electrodes (11) of the chip (10) and are coupled to selected ones of the internal electrodes (11). The larger electrodes (13) permit the conducting leads (21) of the package (20) to project into the interior of the package (20) and be applied directly to the smaller electrodes (11) when the package (20) is assembled. The electrodes (13) and the package leads (21) are wetted with an appropriate preferably solder type alloy (22) to permit convenient electrical coupling.

The electrodes and the package leads are properly shaped, to make the assembly process not dependent on the area.

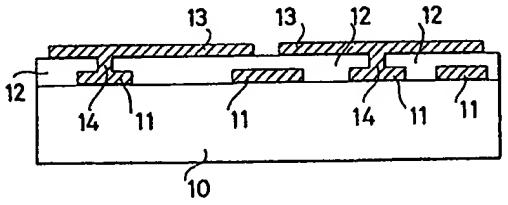
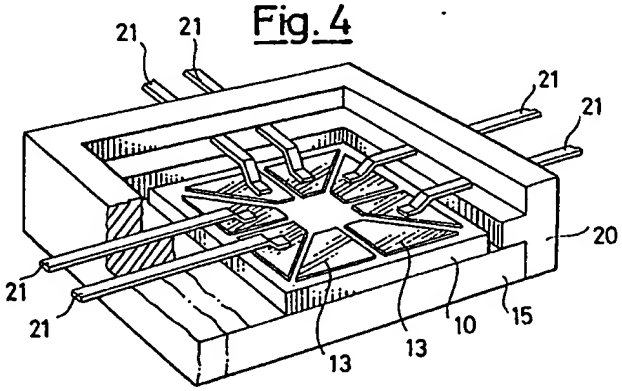


Fig.1

Fig.4



GB 2 174 543 A

2174543

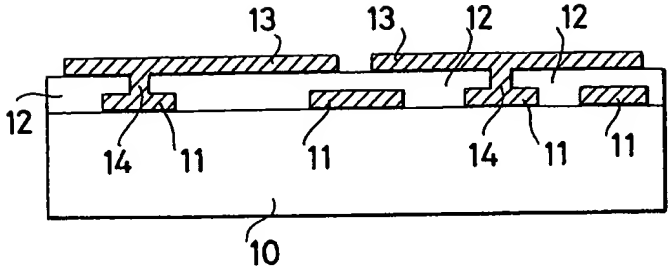


Fig.1

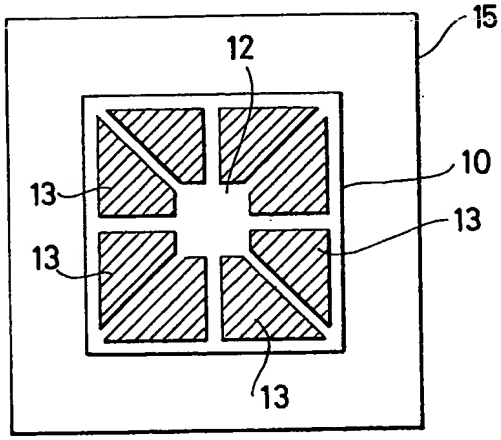


Fig.2

Fig.3

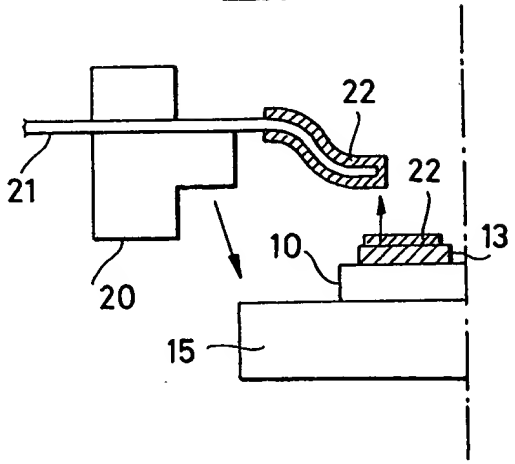
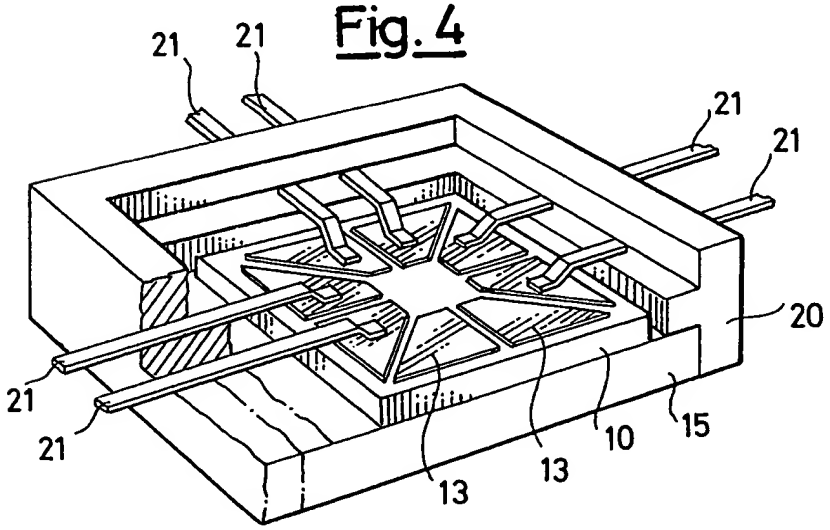


Fig.4



SPECIFICATION

Apparatus and method f r impr ved packaging f semiconductor devices

This invention relates generally to semiconductor device packaging and, more particularly, to the packaging of semiconductor devices such as integrated circuits to permit convenient coupling of a semiconductor device or integrated circuit to leads extending from a package containing the semiconductor device or integrated circuit.

As semiconductor devices of the discrete type or integrated circuit fabricated in semiconductor chips have become more complex and have achieved increasing densities of components, the difficulty of coupling the chips, on which the integrated circuits are fabricated, to the circuits utilizing the integrated circuit components has increased. A typical mechanism for providing an interface between the integrated circuit chip and an electronic circuit is to first place the integrated circuit chip in a package and then bond tiny wire conductors between selected portions of the chip to selected portions of the package. The package has leads extending therefrom that are suitable for coupling for example by means of a printed circuit board to an electronic circuit or system. For example, the package (with leads) can be inserted into via holes in a printed circut board or in a socket in an electrical circuit. However, the electrical coupling from the integrated circuit chip to the package leads has been typically accomplished with fine wire conductors. These fine wire conductors are fragile and have proven relatively difficult to attach between conducting regions of the semiconductor chip and the leads of the package. Furthermore, the top surface of the chip that contained pads for electrical contact to various devices or semiconductor regions of the chip did not provide much flexibility for permitting ease of contact with various leadframe package sizes which was especially important when the size of the chip was either increased or decreased, as needed.

A need was therefore felt for a technique of more securely and reliably coupling the electrically conducting leads of the package directly to the conducting regions of the semiconductor device or integrated circuit chip, thereby producing a strengthened electrical coupling and making the electrical interconnection easier to accomplish.

It is therefore an object of the present invention to provide an improved semiconductor device or integrated circuit packaging technique and method.

It is another object of the present invention to permit an improved coupling between the electrodes of an integrated circuit chip and the conducting leads of a packaging element.

It is a more particular object of the present invention to provide an improved package and method which utilizes the combination of enlarged pad areas of a chip and bent end lead portions of the leadframe package to make more reliable electrical contacts between the leads of the leadframe and the enlarged pad areas of the chip.

It is still further object of this invention to reduc package costs by providing the combination of enlarged pad areas of a chip and bent end lead portions of the leadframe package t permit various sizes of chips to be used with the same package.

It is another particular object of the present invention to provide a procedure for directly applying package leads to an integrated circuit chip.

It is still another particular object of the present invention to provide a direct contact between conducting leads of a package and electrodes of an integrated circuit chip, wherein the conducting leads and electrodes can be coated with a material for easy electrical interconnection.

The aforementioned and other objects are accomplished, according to the present invention, by providing an integrated circuit chip with a layer of insulating material, and depositing a set of relatively large electrodes on the layer of insulating material. The larger electrodes are coupled to integrated circuit electrodes, and the larger electrodes are configured so that the conducting leads of the package supporting the integrated circuit chip are in mechanical contact when the elements of the package as assembled. The package leads and the large electrodes are preferably coated with an appropriate wetting or solder type compound for convenient electrical and mechanical coupling of those elements and electrodes.

According to one embodiment of the present invention, the method of coupling electrodes of a semiconductor chip to leads of a package containing the semiconductor chip comprises the step of depositing large electrodes electrically coupled to preselected electrodes of the semiconductor chip onto an insulating layer, the insulating layer being located over and protecting the chip's electrodes except for the portion of the electrodes extending through the insulating layer into contact with the large electrodes, the large electrodes directly contacting the package leads. At least one of the package leads and the large electrodes are coated with an alloy that melts at a relatively low temperature. The package leads are electrically and mechanically joined to the large electrodes by heating the alloy to cause it to flow and wet and join the large electrodes to the package leads.

According to another embodiment of the present invention, an electronic package is described comprising an integrated circuit chip having a first set of electrodes contacting semiconductor regions of the chip. The chip having a second larger set of electrodes positioned on an insulating material covering the integrated circuit chip except for electrode portions that extend from the first set of electrodes through the insulating layer into contact with the second larger set of electrodes. A package is provided having conducting leads attached thereto. Solder means are provided f r electrically and mechanically connecting the conducting leads to the second set of electrodes.

According to yet another embodiment of the present invention, an apparatus for coupling an integrated circuit chip to an electrical circuit is described comprising conducting means having

portions thereof for electrically coupling to the electrical circuit and package means for supporting the conducting means and the integrated circuit chip. The integrated circuit chip having enlarged electrode means for providing enlarged electrode means for permitting electrical contact to the integrated circuit chip. The conducting means have other portions thereof for providing electrical and mechanical contact to the enlarged electrode means. Solder means are provided for electrically and mechanically coupling to other portions of the conducting means to the enlarged electrode means.

According to yet another embodiment of the present invention, a method of electrically coupling a semiconductor chip to leadframe portions is disclosed. The method includes providing enlarged electrodes on the semiconductor chip, providing bent ends to the leadframe portions, and positioning the semiconductor chip in a package including the leadframe portions so that the bent ends of the leadframe portions and the enlarged electrodes are in contact.

These and other features of the instant invention will be understood by reading the following description along with the figures.

Figure 1 is a cross-sectional view of a semiconductor or integrated circuit chip assembly.

Figure 2 is a top view of the chip assembly of Figure 1 and including a substrate portion to which the chip assembly is preferably attached.

Figure 3 is a cross-sectional view of a portion of the chip assembly/substrate structure of Figure 2 and a portion of a leadframe structure to be attached to the chip assembly.

Figure 4 is a perspective view of a leadframe type of package frame and the chip assembly/substrate structure with part of the package broken away to show the interrelationship of the completed packaged device.

Referring to Figure 1, a semiconductor or preferably integrated circuit chip 10 is shown according to the present invention. The integrated circuit itself is formed in the chip 10. A first level of electrodes or metallization 11 includes a plurality of conductors used to electrically connect to various semiconductor regions to the integrated circuit. Some of the conductors or electrodes 11 of the first level of metallization require electrical coupling to the conducting leads of a lead-frame type of package or frame assembly. Covering the conductors of the first level of metallization 11 is an insulating coating 12 such as silicon dioxide or any suitable deposited insulating material. Next, a second level of metallization 13 is deposited and patterned on the insulating coating 12. The second level of metallization 13 contains a group of enlarged electrodes and is further electrically coupled, through areas or portions 14 passing through the insulating coating 12 to selected or predetermined electrodes 11 of the integrated circuit in th first level of metallization. The group of enlarged electrodes facilitates contact to the leadframe leads and also permits the leadframe leads to contact the enlarged electrodes or pads even if the chip size in increased or decreased (since only the contact region between the leads of the leadframe and the enlarged pads would change with the changing size of the chip, but electrical contact would still be achieved because of the enlarged pads). The various semiconductor regions (N or P type) of the semiconductor chip 10 are not shown, but would be contacted by the electrodes 11.

Referring next to Figure 2, a top view of the chip 10 containing the integrated circuit is shown. Visible are the enlarged electrodes 13 of the second level of metallization preferably formed as either sectors-one for each of eight pins) and the underlying insulating coating 12. The semiconductor chip 10 is shown as being located on a tab or substrate portion 15.

Referring next to Figure 3, the relative positioning of the substrate portion 15 and the chip 10 in a package assembly is shown by depicting a portion thereof to disclose the interconnecting technique of this invention. Walls 20 of the package have electrically conductive leads or leadframe portions 21 passing therethrough. On the interior of the package, the leads 21 are bent or formed with bent end portions to contact the enlarged electrodes 13 of the second level of the metallization, when the chip/substrate assembly is positioned in the package. In addition, the enlarged electrodes 13 of the second level of metallization and the leads 21 associated with the package both preferably have a lead-tin compound or alloy coating or layer 22 affixed thereto or coated thereon.

Referring to Figure 4, a cutaway perspective view of the completed device is shown. When the chip assembly and substrate is in place in the package frame, the leads 21, which are attached to and pass through frame 20, have bent end portions to physically contact the enlarged electrodes 13 of the second level of metallization. Preferably, the bent end portions of the leads 21 are formed prior to the positioning of the chip 10 within the package, but, if desired, the bent end portions of the leads 31 can be formed after the chip 10 is placed within the package. Furthermore, if desired, the substrate 15 can be part of the package and the chip 10 can be placed thereon and preferably secured thereto.

An integrated circuit package must have leads of acceptable durability for attaching to conducting regions of the circuit in which they are to be used, for example, in a socket of a circuit board. In the typical assembly, an integrated circuit chip will have wires, electrically coupled to the electrodes located in a first level of metallization, and electrically coupled to the electrically conductive leads of the package. These prior art type of wires attached to the integrated circuit chip are typically fragile and difficult to attach. The instant invention solves this electrical coupling problem by using enlarged electrodes formed in a second level of metallization containing conductors/electrodes with larger areas than the chip's conductors/electrodes located in the first level of metallization. The leads of the package are placed in direct physical and electrical contact with the enlarged conductors/electrodes f the second level of metallization. Because of the

size of these enlarged electrodes, various sized chips can be used with the same package and the delicate connection problems resulting from the electrical coupling of the small wire leads of the typical prior art assembly are circumvented. In addition, the electrodes of the second level of metallization, as well as the frame leads inside the frame have a lead/tin (such as 90% lead- 10% tin or 95% lead- 5% tin) compound or alloy coating on the surface of each. When the conductors/ electrodes and the frame leads are in contact, a modest amount of heat can be applied (such as by placing the package in a furnace and heating the interior of the furnace to a temperature sufficient to achieve the liquification of the solder coating) resulting in a flow of the solder and in the subsequent formation after cooling of the solder and the wetting of the contacted regions (the bend end portions of the leads 21 with the enlarged electrodes 13) of a good electrical contact, as well as a strengthened mechanical coupling.

Thus an efficient and structurally sturdy method of coupling a semiconductor or integrated circuit chip to leads of a package can be accomplished. The result is an improvement in the ability to reliably interface electrically between a semi-conductor or integrated circuit chip and an external electrical circuit.

The above description is intended to illustrate the operation of the preferred embodiment and is not meant to limit the scope of the invention. The scope of the invention is to be limited only by the following claims. From the above discussion, many variations will be apparent to one skilled in the art that would yet be encompassed by the spirit and scope of the invention.

CLAIMS

1. A method of coupling electrodes of a semiconductor chip to leads of a package containing said chip, characterized by comprising the steps of:

depositing large electrodes (13) electrically coupled to preselected electrodes (11) of said chip (11) onto an insulating layer (12), said insulating layer (12) being located over and protecting said integrated circuit chip electrodes (11) except for the portion of the electrodes (11) extending through the insulating layer (12) into contact with said large electrodes (13), said large electrodes (13) directly contacting said package leads (21);

coating at least one of said package leads (21) and said large electrodes (13) with an alloy (22) that melts at a relatively low temperature; and

electrically and mechanically joining said package leads (21) to said large electrodes (13) by heating said alloy (22) to cause it to flow and wet and join said large electrodes (13) to said package (20).

2. The method of claim 1 wherein said coating step comprises the step of coating both said package leads (21) and said large electrodes (13) with said alloy (22).

3. An electronic package characterized by comprising:

an integrated circuit chip (10) having a first set of electrodes (11) contacting semiconductor regions of said chip (10), said chip (10) having a second larger set of electrodes (13) positioned on an insulating material (12) covering said integrated circuit chip (10) except for electrode portions that extend from the first set of electrodes (11) through said insulating layer (12) into contact with said second larger set of electrodes (13);

a package (20) having conducting leads (21) attached thereto; and

solder means (22) for electrically and mechanically connecting said conducting leads (21) to said second set of electrodes (13).

4. The electronic package of claim 3 wherein said solder means (22) is a lead-tin solder.

5. Apparatus for coupling an integrated circuit chip to an electrical circuit characterized by comprising:

conducting means (21) having portions thereof for electrically coupling to said electrical circuit;

package means (20) for supporting said conducting means (21) and said integrated circuit chip (10), said integrated circuit chip (10) having enlarged electrode means (13) for permitting electrical contact to said integrated circuit chip (10), said conducting means (21) having other portions thereof for providing electrical and mechanical contact to said enlarged electrode means (13) when said integrated circuit chip (10) is coupled to said package means (20); and

solder means (22) for electrically and mechanically coupling said other portions of said conducting means (21) to said enlarged electrode means (13).

6. The apparatus of claim 5 wherein said integrated circuit chip (10) is coupled to a substrate member (15), said substrate member (15) being coupled to said package means (20).

7. The apparatus of claim 5 wherein said conducting means (21) is a lead frame and said enlarged electrode means (13) is attached to said leadframe.

8. The apparatus of claim 7 wherein the leads (21) of said leadframe extend into an interior of said package means (20).

9. The apparatus of claim 5 wherein said other portions of said conducting means (21) having a bent end portion, and end portion of said bent end portion being in mechanical and electrical contact with said enlarged electrode means (13).

10. A method of electrically coupling a semiconductor chip to leadframe portions comprising the steps of:

providing enlarged electrodes (13) on said semiconductor chip (10);

providing bent ends to said leadframe portions (21); and positioning said semiconductor chip (10) in a package (20) including said leadframe portions (21) so that said bent ends of said leadframe portions (21) and said enlarged electrodes (13) are in contact.

Printed in the UK for HMSO, D8818935, 9/86, 7102.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.